WHAT IS CLAIMED IS:

1. A shift register comprising X stages having outputs, where X is an integer greater than three, and Y clock inputs, where Y is an integer greater than two, each xth one of said stages, for each x such that $1<x\leq X$, comprising a flip-flop and logic circuit arranged to receive a set enable signal from said output of an (x-1)th one of said stages, each (nY+y)th one of said stages being arranged to be set in response to one of a leading edge and a first level of a clock signal at a yth one of said clock inputs in a presence of said set enable signal and to be reset in response to one of a trailing edge and a second level of said clock signal at said yth clock input for each y such that $O<y\leq Y$ and where n is a non-negative integer.

2. A register as claimed in claim 1, comprising a start pulse input and in which a first of said stages is arranged to receive a start pulse from said start pulse input.

3. A register as claimed in claim 1, in which each of said flip-flop and logic circuits comprises a reset-over-set flip-flop circuit.

4. A register as claimed in claim 3, in which said reset-over-set flip-flop circuit comprises: a reset-set flip-flop having a set input; and an AND gate having an output connected to said set input of said flip-flop, a first input connected to a yth one of said clock inputs and a second input connected to said output of said (x-1)th stage.

5. A register as claimed in claim 3, in which said reset-over-set flip-flop circuit has a complementary reset input connected to said yth clock input.

6. A register as claimed in claim 1, in which each of said stages comprises a level shifter for shifting a level of a reset signal.

7. A register as claimed in claim 1, comprising a clock signal generator having Y multiphase outputs connected to said Y clock inputs, respectively.

8. A register as claimed in claim 7, in which said clock signal generator is arranged to supply multiphase clock signals with said clock signals of pairs of adjacent ones of said phases overlapping each other.

9. A register as claimed in claim 8, in which said clock signals of non-adjacent ones of said phases are non-overlapping.

10. A register as claimed in claim 1, in which each said xth stage is arranged to receive a set enable signal from said (x+1)th one of said stages.

11. A register as claimed in claim 10, comprising a start pulse input and in which an Xth one of said stages is arranged to receive a start pulse from said start pulse input.

12. A register as claimed in claim 4, in which said reset-over-set flip-flop circuit comprises an OR gate having an output connected to said second input of said AND gate and inputs connected to said output of said (x-1)th stage and to an output of an (x+1)th one of said stages.

13. A register as claimed in claim 7, in which said clock signal generator is controllable to supply clock pulses in sequence to one of said 1st to Yth clock inputs, respectively, and to said Yth to 1st clock inputs, respectively.

14. A register as claimed in claim 7, in which said clock signal generator is controllable to supply inactive clock signals simultaneously to said clock inputs.

15. A register as claimed in claim 7, in which said clock signal generator is controllable to supply active clock signals simultaneously to said clock inputs.

16. A register as claimed in claim 1, comprising an arrangement for converting overlapping output pulses from said stages to non-overlapping pulses.

17. A register as claimed in claim 16, in which said arrangement comprises: a pulse generator for producing timing pulses, each of which has a rising edge after a rising

edge of a respective one of said output signals of said stages and a falling edge before a falling edge of said respective output signal; and X logic circuits, each xth of which is arranged to perform a logical AND operation on said output signal of said xth stage and said timing pulses.

18. A register as claimed in claim 17, in which said rising edge of each said timing pulse occurs after a falling edge of one of said output signals preceding said respective output signal and said falling edge of each said timing pulse occurs before a rising edge of another of said output signals following said respective output signal.

19. A register as claimed in claim 16, in which each of said stages has direct and inverted outputs and said arrangement comprises a plurality of logic circuits, each xth of which is arranged to perform a logical AND operation on said direct output of said xth stage and said inverted outputs of said (x-1)th and an (x+1)th one of said stages.

20. A register as claimed in claim 16, in which each of said stages has direct and inverted outputs and said arrangement comprises a plurality of logic circuits, each xth of which is arranged to perform a logical AND operation on said direct output of said xth stage and said inverted output of one of said (x-1)th and an (x+1)th one of said stages.

21. A register as claimed in claim 1, comprising an arrangement for converting output pulses from the stages to groups of simultaneous pulses.

22. A register as claimed in claim 21, in which said arrangement comprises: a pulse generator for producing timing pulses, each of which overlaps with said output pulses of a respective group of said stages; and X logic circuits, each xth of which is arranged to perform a logical AND operation on said output pulse of said xth stage and said timing pulses.

23. A register as claimed in claim 22, in which a rising edge of each said timing pulse occurs after rising edges of all said output signals of said respective group and a falling edge of each said timing pulse occurs before falling edges of all of said output signals of said respective group.

24. A register as claimed in claim 1, in which Y is equal to three.

25. A register as claimed in claim 1, in which each of said clock inputs is a complementary clock input for receiving complementary clock signals.

26. A register as claimed in claim 1, comprising a CMOS integrated circuit.

27. A driver for an active matrix device, said driver comprising a shift register comprising X stages having outputs, where X is an integer greater than three, and Y clock inputs, where Y is an integer greater than two, each xth one of said stages, for each x such that $1<x\leq X$, comprising a flip-flop and logic circuit arranged to receive a set enable signal from said output of an (x-1)th one of said stages, each (nY+y)th one of said stages being arranged to be set in response to one of a leading edge and a first level of a clock signal at a yth one of said clock inputs in a presence of said set enable signal and to be reset in response to one of a trailing edge and a second level of said clock signal at said yth clock input for each y such that $O<y\leq Y$ and where n is a non-negative integer.

28. An active matrix device including at least one driver comprising a shift register comprising X stages having outputs, where X is an integer greater than three, and Y clock inputs, where Y is an integer greater than two, each xth one of said stages, for each x such that $1<x\leq X$, comprising a flip-flop and logic circuit arranged to receive a set enable signal from said output of an (x-1)th one of said stages, each (nY+y)th one of said stages being arranged to be set in response to one of a leading edge and a first level of a clock signal at a yth one of said clock inputs in a presence of said set enable signal and to be reset in response to one of a trailing edge and a second level of said clock signal at said yth clock input for each y such that $O<y\leq Y$ and where n is a non-negative integer.

29. A device as claimed in claim 26, comprising a liquid crystal display.